UNITED STATES DEPARTMENT OF COMMERCE
Pat nt and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/725,862	11/30/00	GRECO S	00750414BA

MMC2/0801

MCGUIRE WOODS, LLP
SUITE 1800
1750 TYSONS BLVD.
MCLEAN VA 22102-4215

EXAMINER	
NGUYEN, J	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/01/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/725,862	GRECO ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 27-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 27-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 November 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of claim 31 "a supplemental protective layer on said primary protective layer" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

The disclosure is objected to because of the following informalities: on page 16, line 14, "3740" should be --"37- 40"--. Also, on page 12, lines 4 –5, "were extrusion a concern in the structure" is grammar error. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Bai et al.

Regarding claim 27, Bai et al discloses an integrated circuit semiconductor device including "a substrate [40] having a substrate surface [readable on figure 4D], a flowable oxide insulator layer [41] upon said substrate surface; a trough [44], sidewalls [43,42] of said flowable oxide insulator layer [41], a primary protective layer [43] on said

sidewalls of said flowable oxide insulator layer [41], said primary protection layer preventing the exposure of said flowable oxide insulator layer to moisture and lithographic resist developers, said primary protective layer [43] being impervious to copper extrusion, and a secondary protective layer [42] on said primary protection layer and on said substrate surface, said secondary protective layer [42] being electrically conductive [col. 8, line 40]". This is all illustrated in figure 4D.

Claims 27, 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Lopatin et al.

Regarding claim 27, Lopatin et al discloses an integrated circuit semiconductor device including "a substrate [101] having a substrate surface [readable on figure 2], a flowable oxide insulator layer [116] upon said substrate surface; a trough [102], sidewalls [123,124] of said flowable oxide insulator layer [116], a primary protective layer [123] on said sidewalls of said flowable oxide insulator layer [116], said primary protection layer preventing the exposure of said flowable oxide insulator layer to moisture and lithographic resist developers, said primary protective layer [123] being impervious to copper extrusion, and a secondary protective layer [124] on said primary protection layer and on said substrate surface, said secondary protective layer [124] being electrically conductive [col. 1, lines 31-32]". This is all illustrated in figure 2.

Regarding claim 28, Lopatin et al further discloses "an oxidized FOX layer [117] upon said floatable oxide insulator layer [116], an oxide layer [108] upon said oxidized FOX layer, a conductor [102] in said trough, said conductor and said oxide layer forming

an even planar surface, said conductor being in electrically communication with said secondary protective layer [124], and a nitride layer [126] upon said even planar surface". This is all illustrated in figure 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al as applied to claim 28 above, and further in view of Yew et al.

Regarding claims 29 and 30, Lopatin et al discloses substantially all the structure set forth in the claimed invention except the integrated circuit semiconductor device comprising a second damascene layer. Note that the second damascene layer is merely duplication of the first damascene layer of claim 27. However, Yew et al discloses on figure 2E the second damascene layer 226, 212 similar to the first damascene layer 222, 204. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lopatin et al by having the second damascene layer similar to the first damascene layer in the integrated circuit semiconductor device. The ordinary artisan would have been motivated to modify Lopatin et al in the manner described for the purpose of having a reduced parasite capacitance in the dielectric layers, thus assuring the performance of an IC device (col. 3, line 15-18).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al or Bai et al as applied to claim 27 above, and further in view of Kawanoue et al.

Regarding claim 31, Lopatin et al or Bai et al discloses substantially all the structure set forth in the claimed invention except the integrated circuit semiconductor device comprising a supplemental protective layer on primary protective layer, being impervious to moisture, lithographic resist developers and copper extrusion and improving adhesion with a metallic conductor. However, Kawanoue et al discloses on figure 3C the integrated circuit semiconductor device having a supplemental protective layer 35 on primary protective layer 203, being impervious to moisture, lithographic resist developers and copper extrusion and improving adhesion with a metallic conductor. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lopatin et al or Bai et al by having a supplemental protective layer upon the protective layer, being impervious to moisture, lithographic resist developers and copper extrusion and improving adhesion with a metallic conductor in the integrated circuit semiconductor device. The ordinary artisan would have been motivated to modify Lopatin et al or Bai et al in the manner described for the purpose of achieving a low via resistance, a low interconnect resistance and a high barrier effect in the integrated circuit semiconductor device (col. 10, line 30-36).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6221758 B1 to Liu et al discloses a method of forming a semiconductor device having an electrically conductive substrate covered with a dielectric layer.

US Patent 6222269 B1 to Usami discloses a semiconductor device having a plurality of interconnect lines disposed through an insulating layer on the same layer above a semiconductor substrate.

US Patent 6187663 B1 to Yu et al discloses a process for fabricating a copper damascene structure embedded in two levels of low dielectric constant and composite insulators layers.

US Patent 6163682 to Hegde et al discloses a method for forming an improved copper barrier layer by providing a silicon-containing layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
July 24, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800